layer **30** and the n drain **3** such that the threshold current density becomes higher and reaches 1100 A/cm^2 or the high.

In addition to the above-mentioned advantages that the device can reduce power dissipation, the device can also increase tolerance for destruction thereof when it is short-circuited. During an operation mode where the on-resistance is kept lower by means of the conductivity modulation by the injection of carriers into the drain region **3**, if an accident, e.g. a load (not shown) is short-circuited, takes place, the injection of carriers into the drain region is prevented because a voltage which has an approximately equal potential to a power voltage is applied to the drain region **3** such that the potential thereof becomes extremely higher than that of p^+ semiconductor layer **30**. Accordingly, the conductivity modulation is stopped such that the on-resistance increases. This results in suppressing a current through the semiconductor device, and therefore, the tolerance of device increases.

Furthermore, the various embodiments shown in the drawing can be manufactured with a well-known process for power-MOS devices. The process for the device of the present invention does not require any special steps. The device thereby can be manufactured easily.

As described above, according to the present invention, it is possible to inject the holes into the drain of the voltage-driven type semiconductor device by a bipolar transistor having a very small collector saturation resistance so as to give rise to conductivity modulation in the drain. As a result, the power dissipation of the voltage-driven type semiconductor device can be made very small, and further, when it is assumed that the power dissipation is the same as before, the turn-off time of the voltage-driven type semiconductor device is shortened thereby enabling high-speed operation.

According to the present invention, a remarkable effect of reduction the in power dissipation and an effect of shortening turn-off time are obtainable in the use for high breakdown voltage and large current in particular.

The present invention has been described in detail, but it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the present invention as defined by the appended claims.

We claim:

1. A voltage-driven type semiconductor device comprising:

a first device having a linear volt-ampere characteristic, said first device including a first semiconductor region of first conductivity type said first device being provided with a first electrode applied with drive voltage at a first surface thereof, and having a pair of main electrodes to provide a predetermined voltage across the first semiconductor region;

a second semiconductor region, distinct from the first device, of a second conductivity type located at a position at a distance from said first surface of said first device and for injecting carriers into said first semiconductor region so as to modulate conductivity thereof;

a second electrode coupled to said second semiconductor region,

wherein said second semiconductor region is formed on a plane opposite to said first surface in said first device

wherein said first device portion is comprised of a voltage-driven type transistor, said first semiconductor region is a drain region of said voltage-driven type transistor, said second semiconductor region is a base of a bipolar transistor, and wherein said first and second semiconductor regions have the opposite conductivity type, and are coupled with each other through an emitter region of said bipolar transistor, and

wherein a third semiconductor region for connecting a collector region and said emitter region with each other is provided in the base region of said bipolar transistor, and said third semiconductor region has the same conductivity type as that of said emitter.

2. A voltage-driven type semiconductor device comprising:

a first semiconductor region of a first conductivity type having a pair of main surfaces;

a second semiconductor region of a second conductivity type coupled with one of said pair of main surfaces of said first semiconductor region;

a third semiconductor region of the first conductivity type coupled with said second semiconductor region;

a fourth semiconductor region of the first conductivity type coupled with the other main surface of said first semiconductor region;

a fifth semiconductor region of the second conductivity type coupled with said fourth semiconductor region;

a sixth semiconductor region of the first conductivity type coupled with said fifth semiconductor region;

a gate electrode arranged on a date insulator over a portion of said second semiconductor region between said first semiconductor region and said third semiconductor region;

a first main electrode contacting with said second semiconductor region and said third semiconductor region; and

a second main electrode contacting with said sixth semiconductor region,

wherein said second semiconductor region and said fifth semiconductor region are buried so as to be exposed on the main surface of said first semiconductor region, said third semiconductor region is buried in said second semiconductor region and said sixth semiconductor region is buried in said fifth semiconductor region.

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